Remarks & Arguments

In the Office Action, the Examiner noted that Claims 1-5, 10-14 and 18-20 are pending in the application, Claims 10-14 are allowed, Claims 2, 3, 19 and 20 are objected to, and that Claims 1, 4, 5 and 18 are rejected. The Examiner's rejections are traversed below.

Rejections Under 35 U.S.C. 102

Claims 1, 4, 5 and 18 stand rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent No. 5,444,744 to Yamamoto.

With regard to **Claim 1**, the Office refers to Yamamoto at Figure 8, to support the assertion that Yamamoto teaches "an indicator module (9a, 11, 12, 21) having a first indicator input receiving an input signal (14), a second indicator input for receiving a reference voltage (9b), a third indicator input communicatively coupled to said pulse output (b) of said pulse module (15b) and an indicator output for outputting a pass/fail indicator signal (I) as a function of said stream of reset pulses (B) and a difference between an input signal (14) and a reference voltage (9b)." The applicants respectfully disagree with the Office's position, and suggest that Yamamoto does not support the Office's assertion. First, the Examiner has asserted that Yamamoto discloses an "indicator module" that consists of an operational amplifier 9a, a multiplier 11, a first EX-OR 12 and a second EX-OR 21. The Examiner has identified I4 as a first input signal to the "indicator module," the reference voltage 9b as a second input signal to the "indicator module," the first reference signal as a third input signal to the "indicator module,"

and the negative direction phase difference signal I as output of the "indicator module." However, it is clear from Figure 8 that the negative direction phase difference signal I is not the output of the "indicator module" consisting of devices 9a, 11, 12 and 21. Instead, the phase comparison signal E is the output of the alleged "indicator module" in Yamamoto. Accordingly, the Examiner's arguments are not supported by the portions of Yamamoto that the Examiner relies upon.

In addition, the Examiner attempts to rely upon Figures 10A-10I in Yamamoto and ignore Figures 9A-I and 11A-11I. However, those skilled in the art appreciate that Figures 10A-10I in isolation do not disclose the operation of the circuit in Figure 8, Figures 10A-10I only disclose the state of signals in the circuit in Figure 8 at a particular instant of time. Figures 9A-9I, 10A-10I and 11A-11I must be considered together to illustrate the operation of the circuit in Figure 8 that Yamamoto discloses. When Figures 9A-9I, 10A-10I and 11A-11I are considered together, as described at col. 7, line 13, through col. 8, line 9, the disclosure of Yamamoto clearly refutes the Examiner's interpretation.

The Examiner, in his Response to Arguments, alleges that the recitation "a stream of reset pulses" is merely a label that does not have any specific function. The Applicants assert that every element is "merely a label" when considered in isolation. However, it is well settled law that the claims must be considered as a whole, that the claimed combination must be disclosed in the prior art, and that the limitations are interpreted as it would be interpreted by one of ordinary skill in the art. Those skilled in the art understand that a "stream of reset pulses" perform a reset function. Furthermore, those skilled in the art appreciate, based upon the claimed combination

of "an indicator module having a first indicator input for receiving an input signal, a second indicator input for receiving a reference voltage, **a third indicator input** communicatively coupled to said pulse output [for outputting a stream of reset pulses] of said pulse module and **an indicator output** for outputting a pass/fail indicator signal **as a function of said stream of reset pulses** and a difference between an input signal and a reference voltage," that the stream of reset pulses perform the function of resetting the state of the "indicator module." Thus, those skilled in the art understand that the output of the indicator module is dependent upon the state of the first and second inputs when the reset pulse is in a first state and is independent of the state of the first and second inputs when the reset pulse is in a second state (e.g., reset). In particular, the output of the indicator module is set to a reset state irrespective of the state of the first and second inputs. In contrast, those skilled in the art understand that the output of the multiplier (D-flip-flop) 11 as disclosed in Yamamoto is dependent upon the state of the input A. The clock signal B never drives the output of the D-flip-flop 11 to a state that is independent of the input signal A. Consequently, the clock signal B also never drives the output of the first or second EX-Ors 12, 21 to a state that is independent of the input signal A, input signal (I4), or reference voltage (9b).

The Applicants also respectfully assert that the Examiner's rejection is premised upon modifications of the Yamamoto disclosure and therefore cannot be based upon anticipation, but only obviousness. In particular, the Examiner is modifying the **phase** deviation detection function disclosed by Yamamoto to allegedly teach or suggest a **voltage** deviation detection. In addition, upon comparing Figures 7 and 8, it is clear that the Examiner recombining devices (that

Yamamoto discloses perform specific functions) to instead perform different functions that Yamamoto clear does not disclose, teach or suggest. In particular, the Examiner's allegation to combine the comparator 9a, the multiplier 11, the first EX-OR 12 and a device from the phase detector 13 (the second EX-OR 12) to disclose an "indicator module" is a clear and unequivocal modification of Yamamoto. Similarly, the Examiner's allegation to remove the second EX-OR 12 from the phase detector 13 to disclose a "correlation module" is a clear and unequivocal modification of Yamamoto. In addition, the Examiner is ignoring that there is a feedback path between the output and the input of the Examiner's "correlation module" (the combination of 22, 23, 24 and 25, but excluding 21 and 26) that Yamamoto allegedly discloses. There is also a feedback path between the output and input of the Examiner's "indicator module" (the combination of 9a, 11, 12 and 21) that Yamamoto allegedly discloses. Yet the feedback path, sequential loop filter 14 and variable divider 15b that the Examiner selectively excluded cause the alleged "indicator module" to operate differently from the function that the Examiner alleges. Likewise, the feedback path, sequential loop filter 14, variable divider 15b, multiplier 11 and first and second EX-ORs 12, 21 cause the alleged correlation module to function differently from the function that the Examiner alleges. Thus the Examiner's rejection is premised upon substantial material modifications of the Yamamoto. Therefore, the Examiner has not made a prima facie case in support of the anticipation rejection under 35 U.S.C. 102.

Furthermore, even if the Examiner had properly made an obviousness rejection under 35 U.S.C 103, the rejection fails to establish a prima facie case of obviousness. First, there is no teaching or suggestion to selectively recombine devices 9a, 11, 12 and 21, while removing the

feedback path, sequential loop filter 14, variable divider 15b, multiplier 11, and first and second EX-Ors 12, 21, to form an "indicator module." Likewise, there is not teaching or suggestion to selective recombining devices 22, 23, 24 and 25, while ignoring the inverter 26, the feedback path, the sequential loop filter 14, and variable divider 15b, to form a "correlation module." Second, the Examiner's modifications render the disclosed digital phase lock loop unsatisfactory for its intended purpose. In particular, by selectively omitting the feedback path, sequential loop filter 14 and variable divider 15b, that the circuit modified circuit is incapable of the phase lock function that Yamamoto discloses.

For each of the reasons set forth above, Applicants respectfully submit that the Examiner has failed to make a prima facie case to support the anticipation rejection under 35 U.S.C. 102. In addition, the Examiner's rejection fails to make a prima facie case to support an obviousness rejection under 35 U.S.C. 103. Accordingly, Applicants request that the rejection of Claim 1 be withdrawn and that Claim 1 be allowed.

Claims 4 and 5 are allowable by virtue of their dependency on respective base Claim 1, as well as the additional elements they recite. Accordingly, Applicants respectfully request that the rejection of Claims 4 and 5 be withdrawn and that Claims 4 and 5 be allowed.

With regard to **Claim 18**, Applicants respectfully submit that the Examiner has failed to make a prima facie case to support the anticipation rejection for each of the reasons set forth above with regard to Claim 1. In addition, the Examiner's rejection fails to make a prima facie case to support an obviousness rejection under

35 U.S.C. 103. Accordingly, Applicants request that the rejection of Claim 18 be withdrawn and that Claim 18 be allowed.

Conclusion

For all the reasons advanced above, Applicants respectfully submit that the present application is in condition for allowance and that action is earnestly solicited. The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

The Commissioner is hereby authorized to charge any additional fees, which may be required for this amendment, or credit any overpayment, to Deposit Account 23-0085. In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to Deposit Account 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

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Eric J. Gash
Registration No. 46,274
Tel.: (408) 938-9060